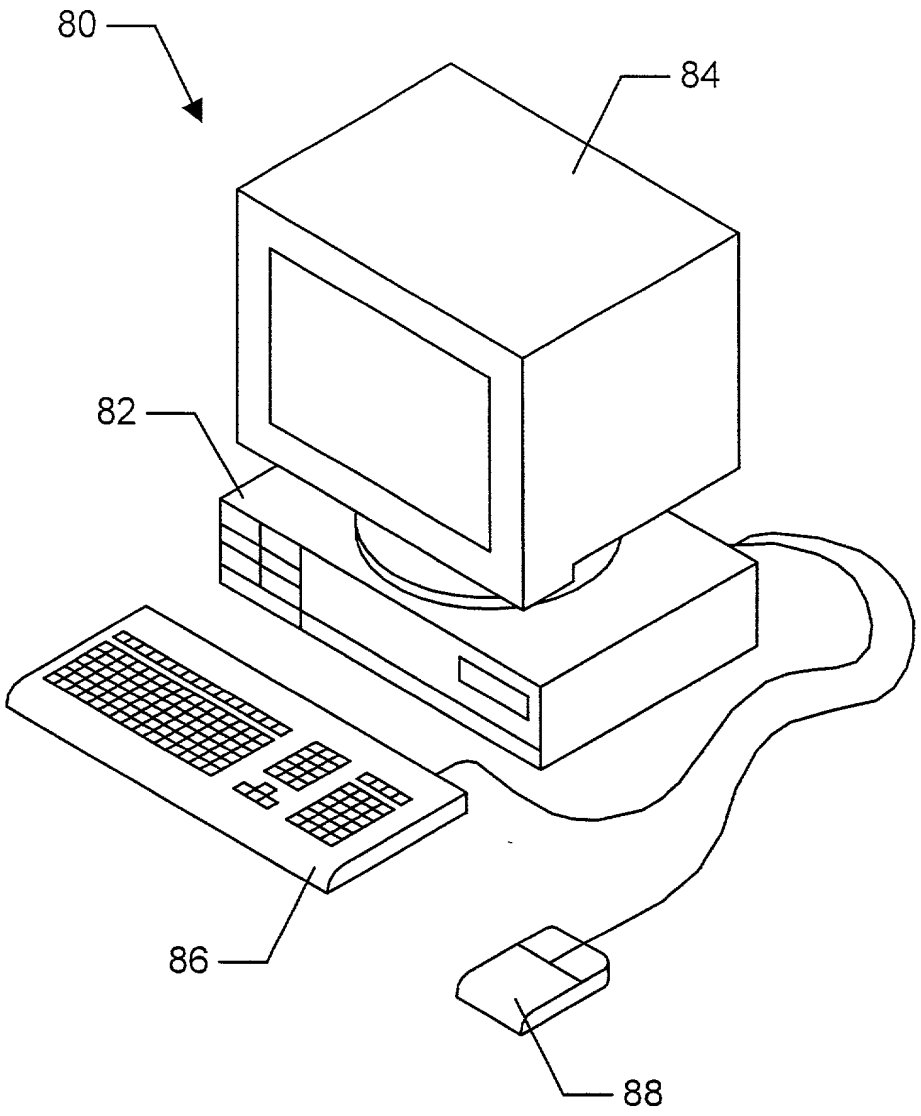

FIG. 1

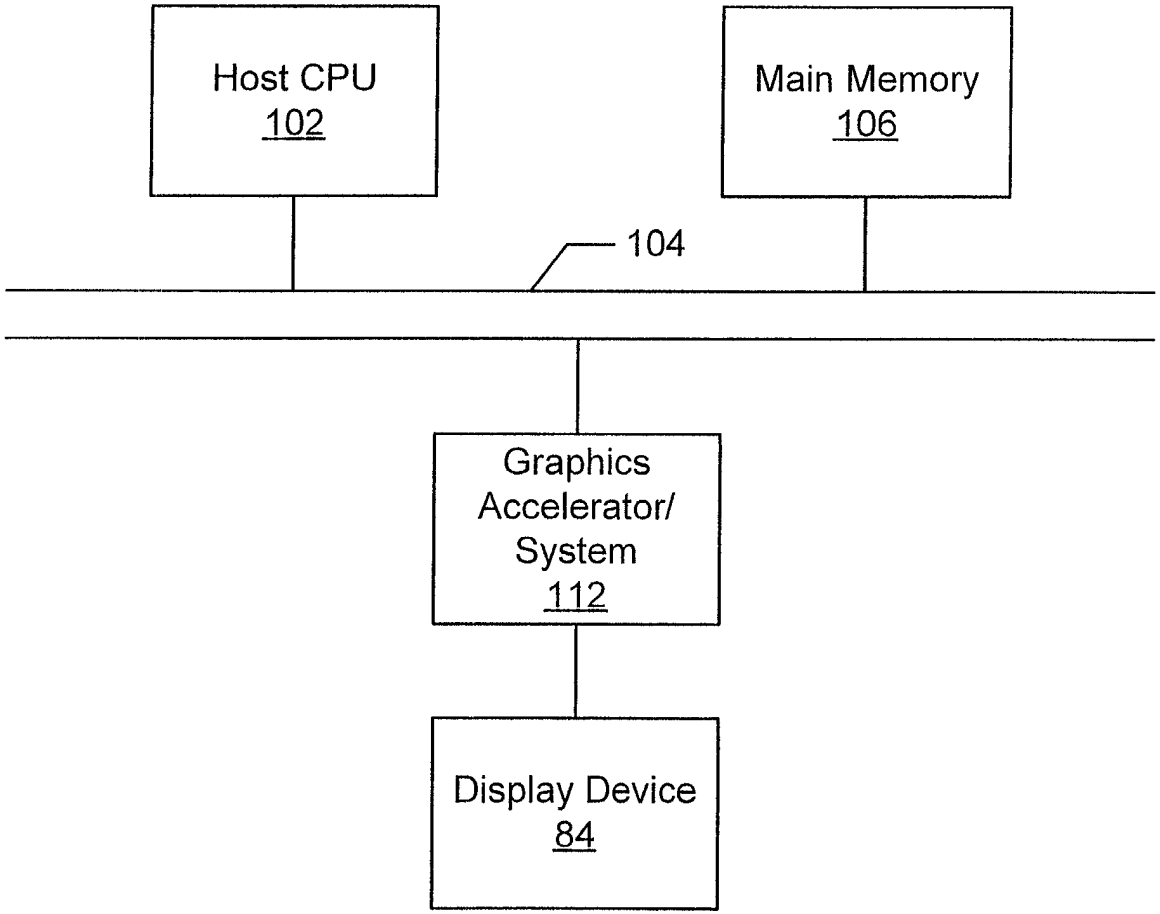
Host CPU
102
Main Memory
106
104
Graphics
Accelerator/
System
112
Display Device
84

FIG. 2

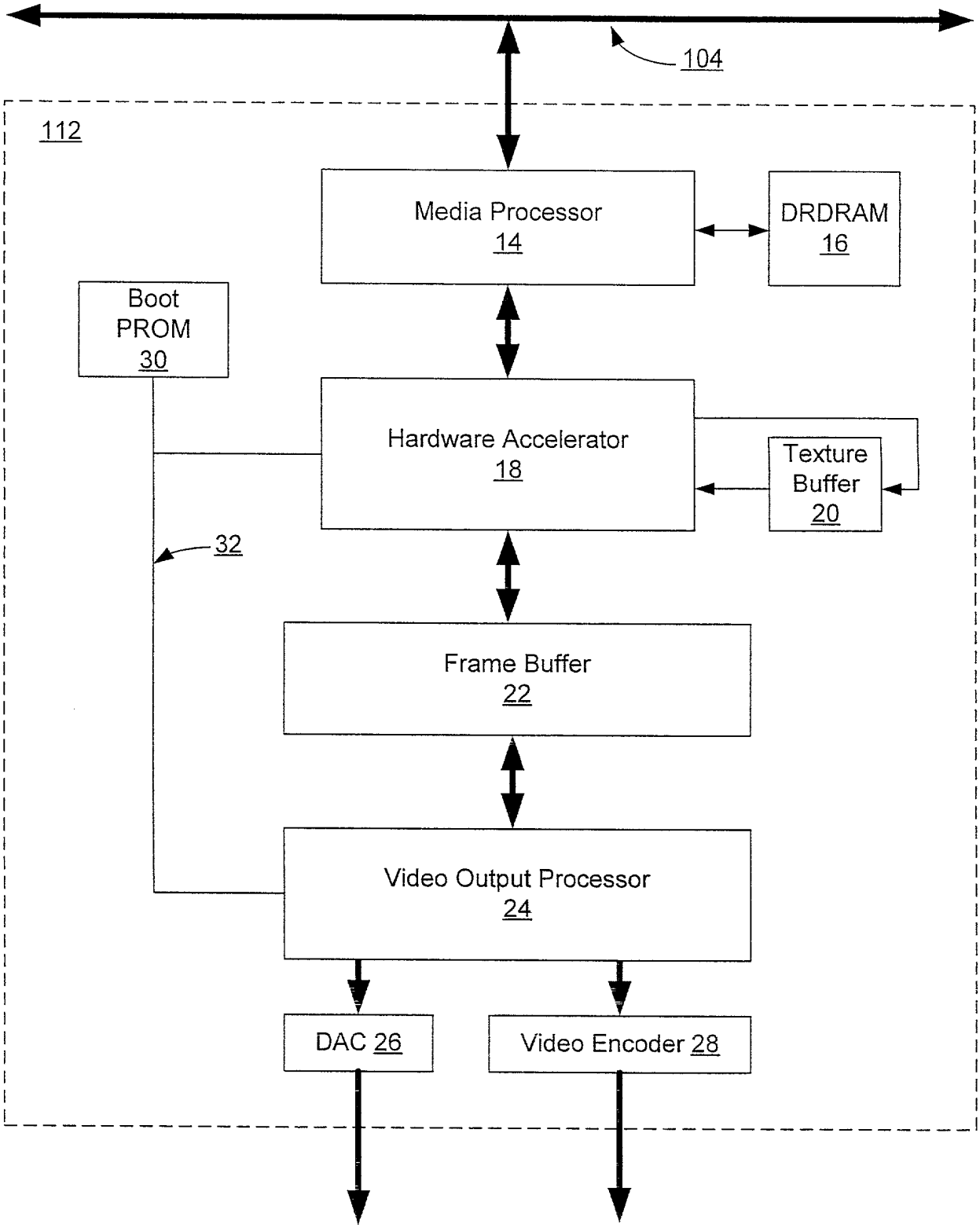
104
112
Media Processor
14
DRDRAM
16
Boot
PROM
30
Hardware Accelerator
18
Texture
Buffer
20
32
Frame Buffer
22
Video Output Processor
24
DAC 26
Video Encoder 28

FIG. 3

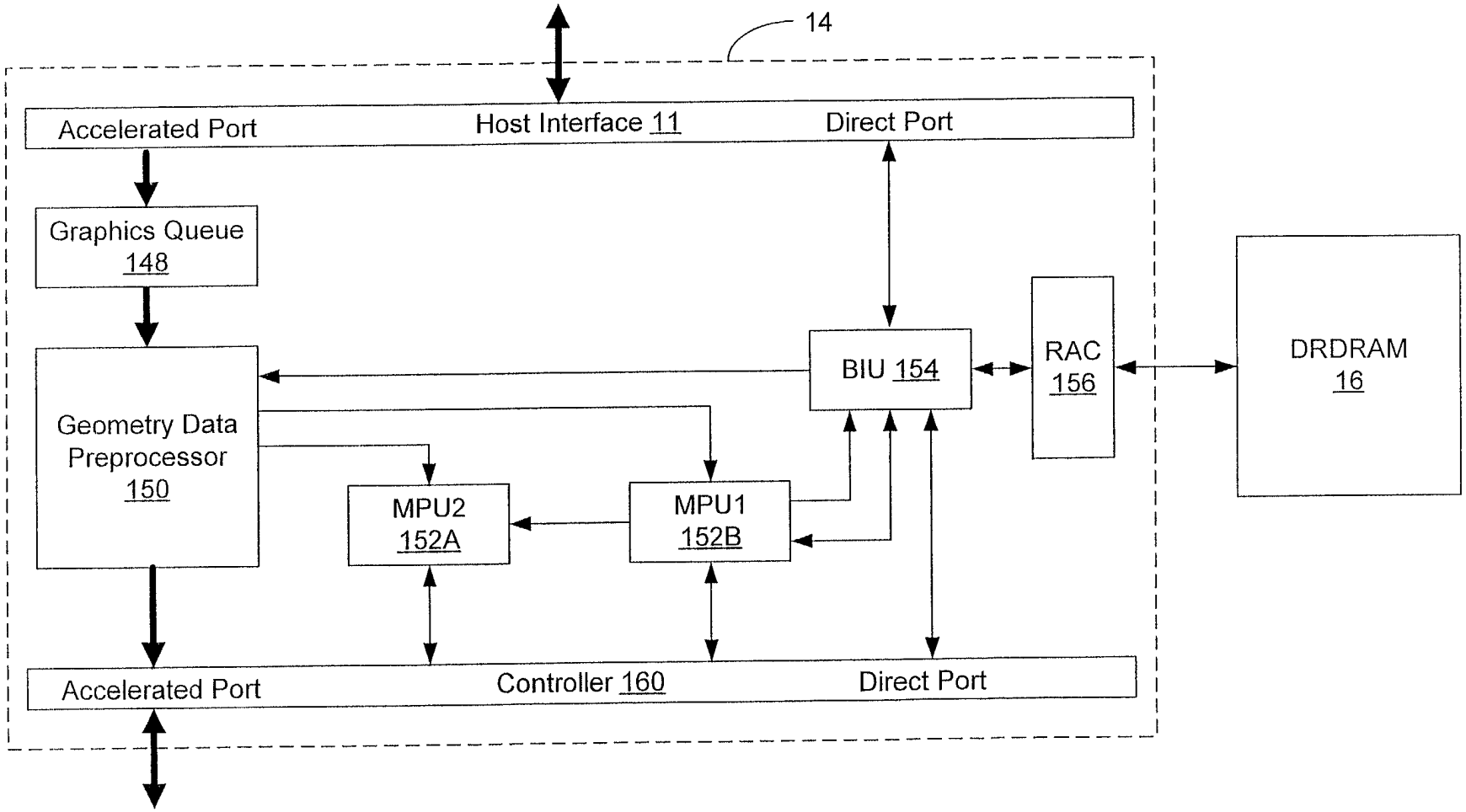
14
Accelerated Port
Host Interface 11
Direct Port
Graphics Queue
148
Geometry Data
Preprocessor
150
BIU 154
RAC
156
DRDRAM
16
MPU2
152A
MPU1
152B
Accelerated Port
Controller 160
Direct Port

FIG. 4

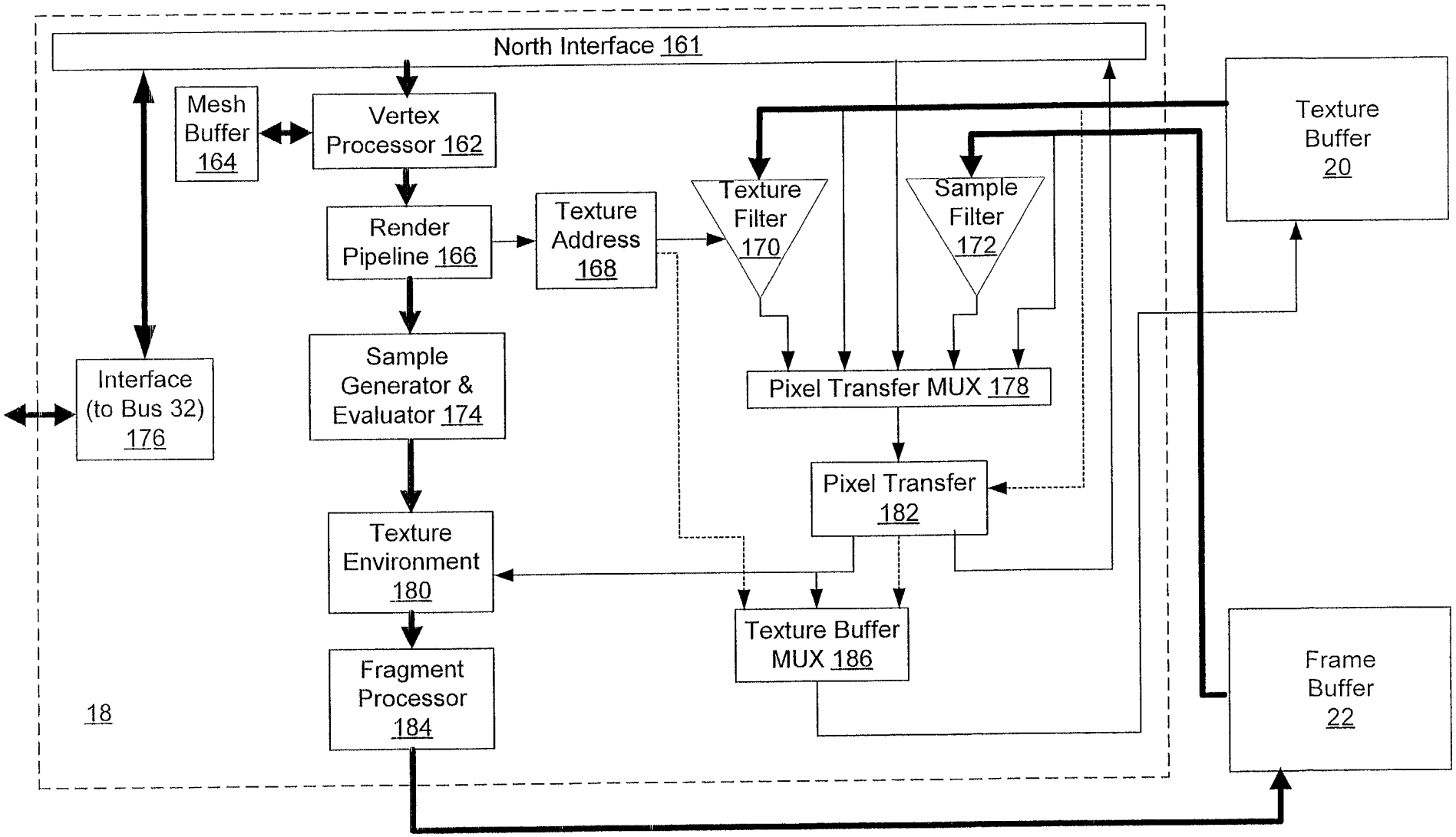
North Interface 161
Mesh Buffer 164
Vertex Processor 162
Render Pipeline 166
Texture Address 168
Texture Filter 170
Sample Filter 172
Texture Buffer 20
Interface (to Bus 32) 176
Sample Generator & Evaluator 174
Pixel Transfer MUX 178
Pixel Transfer 182
Texture Environment 180
Texture Buffer MUX 186
Fragment Processor 184
Frame Buffer 22
18

FIG. 5

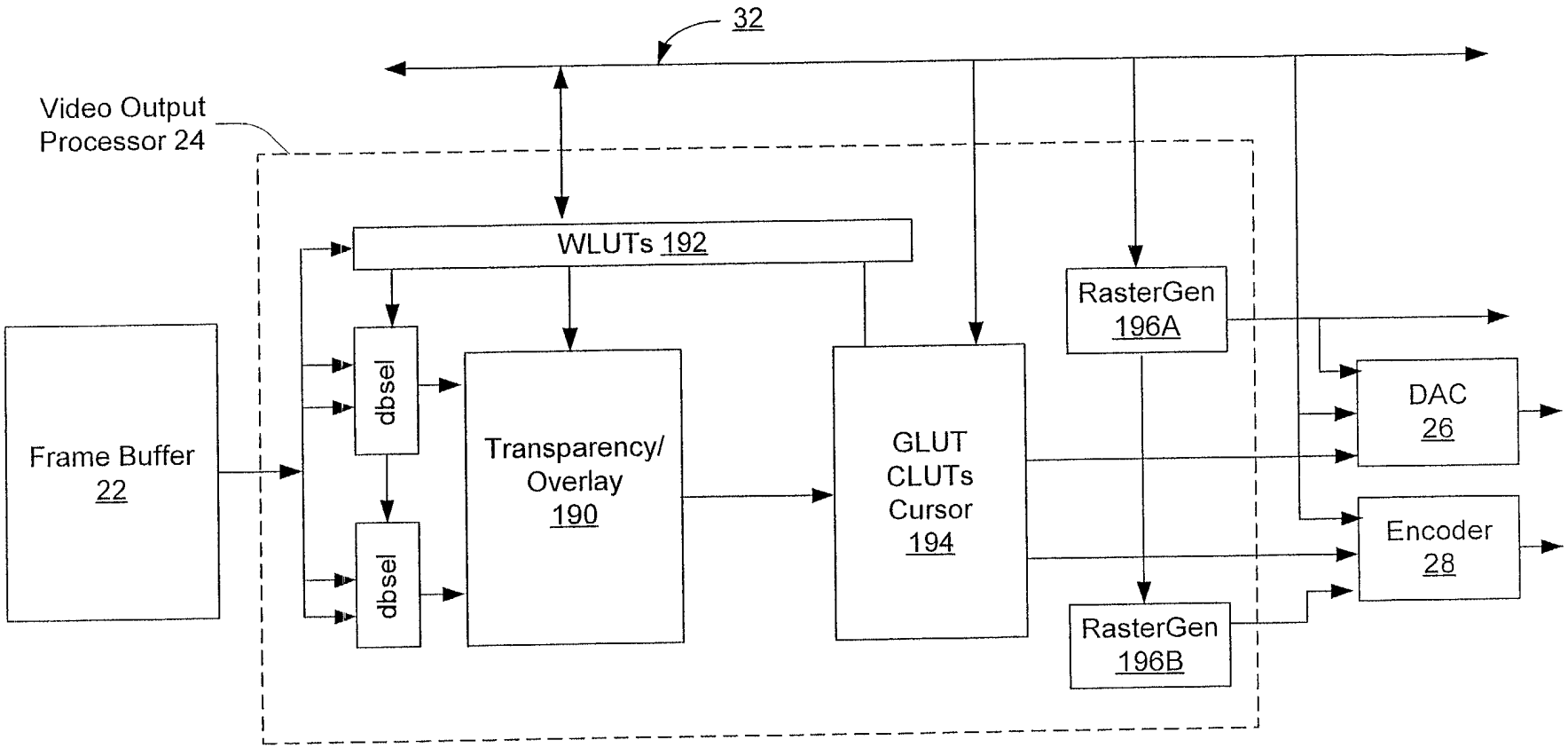
32
Video Output
Processor 24
WLUTs 192
Frame Buffer
22
dbsel
dbsel
Transparency/
Overlay
190
GLUT
CLUTs
Cursor
194
RasterGen
196A
RasterGen
196B
DAC
26
Encoder
28

FIG. 6

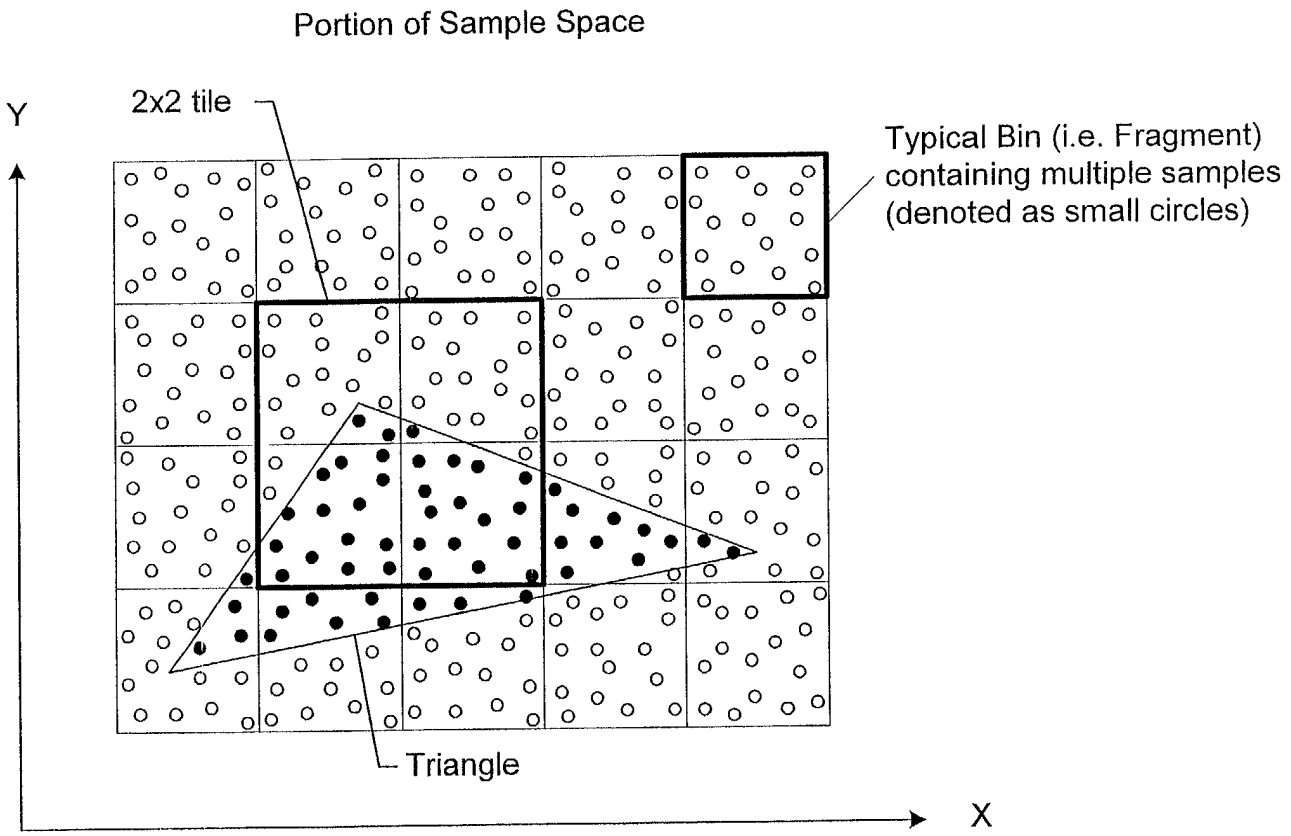
Portion of Sample Space
2x2 tile
Typical Bin (i.e. Fragment)
containing multiple samples
(denoted as small circles)
Y
X
Triangle

Fig. 7

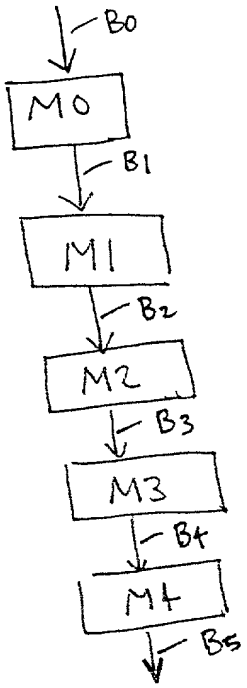

Fig. 8

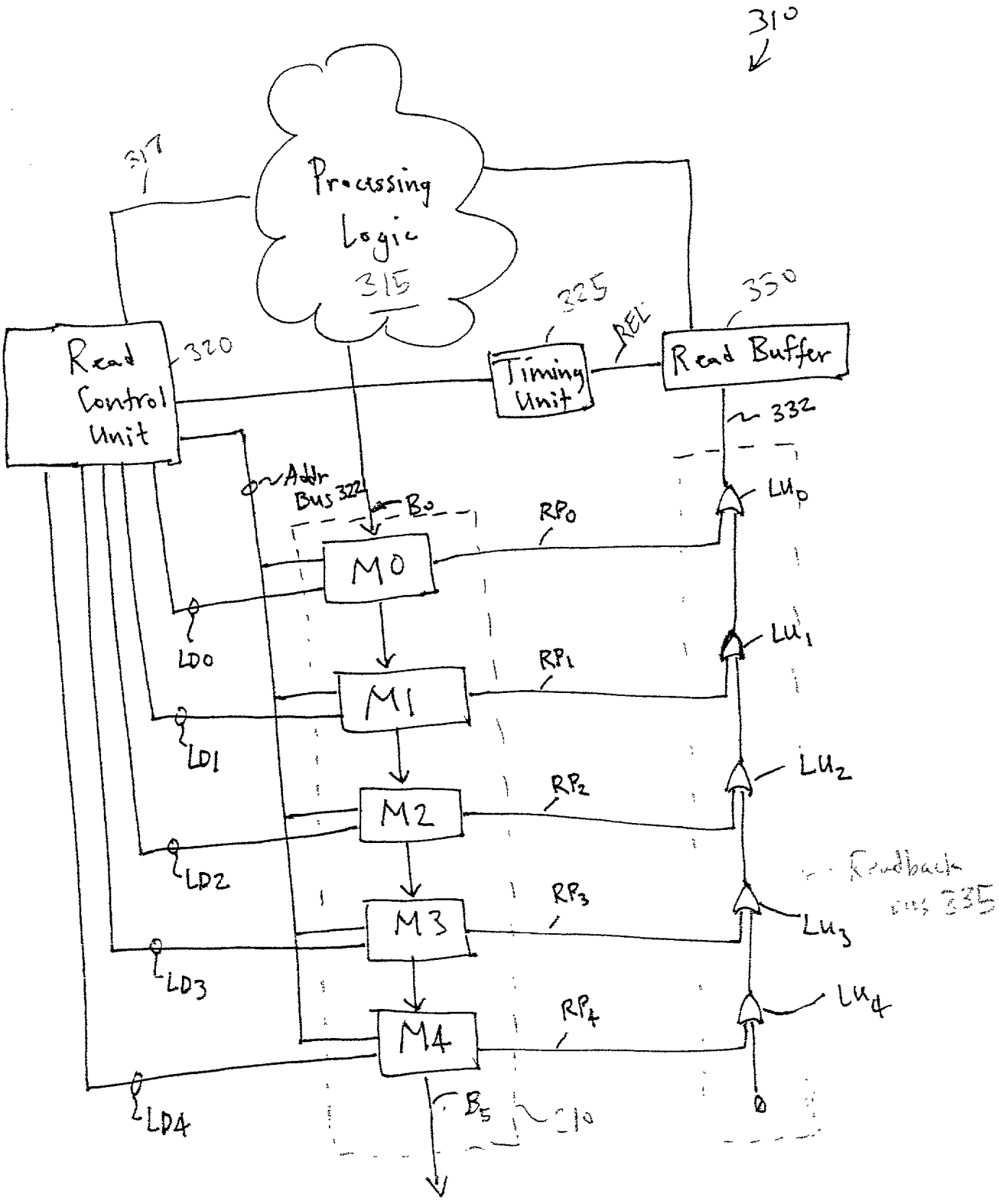
310
317
Processing Logic 315
325
350
REL
Read Control Unit
320
Timing Unit
Read Buffer
332
Addr Bus 322
B0
RP0
LUp
M0
LD0
LU1
RP1
M1
LD1
LU2
RP2
M2
LD2
Readback bus 335
RP3
M3
LU3
LD3
LU4
RP4
M4
B5
310
0
LD4

Fig. 9

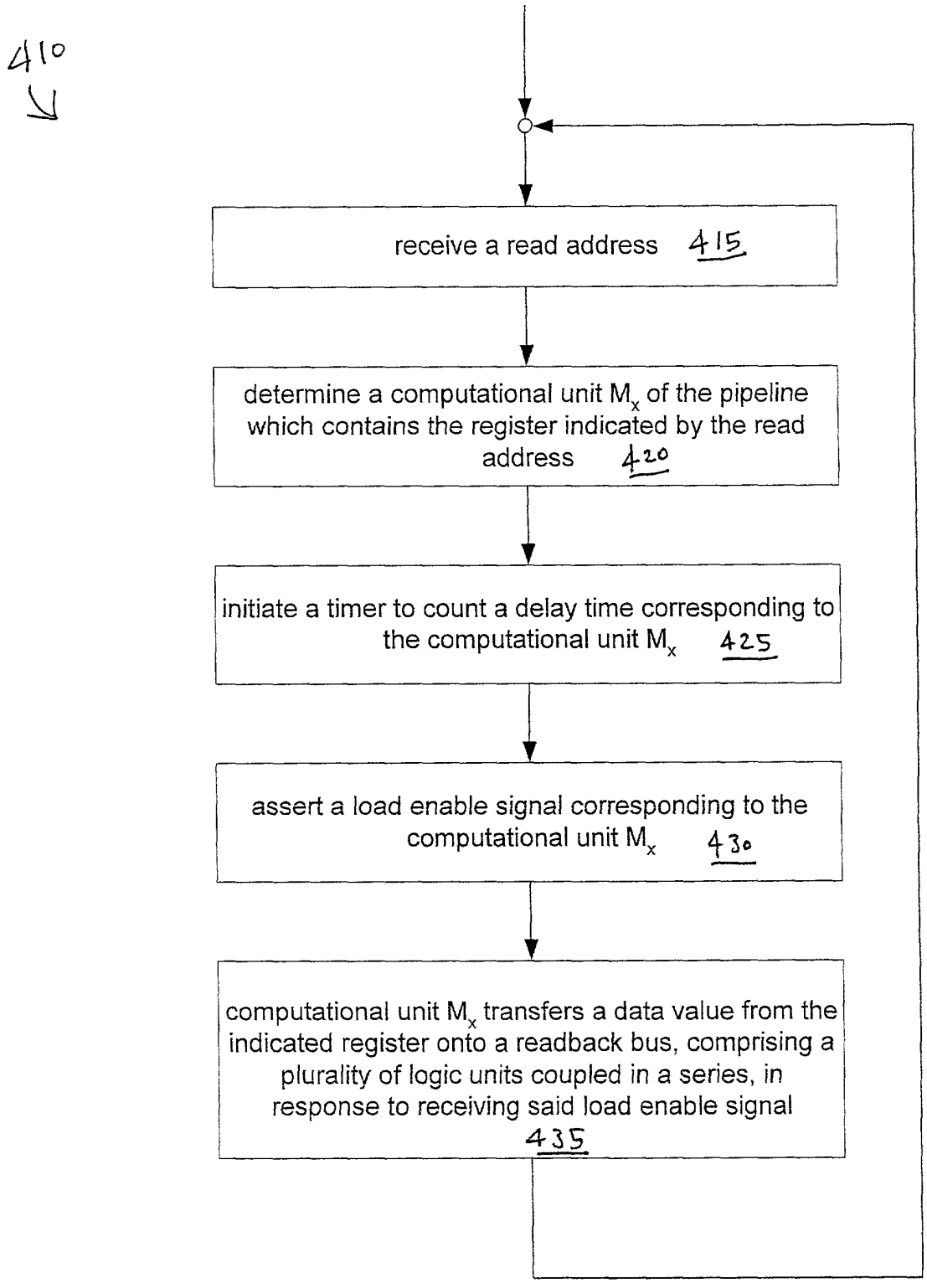
410
receive a read address 415
determine a computational unit M_x of the pipeline which contains the register indicated by the read address 420
initiate a timer to count a delay time corresponding to the computational unit M_x 425
assert a load enable signal corresponding to the computational unit M_x 430
computational unit M_x transfers a data value from the indicated register onto a readback bus, comprising a plurality of logic units coupled in a series, in response to receiving said load enable signal 435

Fig 10